Amendments to the Claims

The listing of claims will replace all prior versions, and listings of claims in the application.

1. (Currently amended) An apparatus comprising:

a shift post processor;

a shifter to shift an operand according to an offset parameter, generating a shifted operand; and

a register coupled to the shift post processor capable of transferring a shift carry operand stored in the register to the shift post processor, and coupled to the shifter to store the shifted operand after any transfer of the shift carry operand;

wherein the shift post processor is coupled to the shifter and the register to process the shifted operand to generate an output based on at least a control signal and a mask field; and

wherein the shift post processor comprises

a decoder to decode the offset parameter into the mask field, the mask field having a plurality of mask bits, each of the mask bits corresponding to a bit position of the shifted operand, and

at least one bit formatter coupled to the decoder to format the shifted operand using the control signal and the mask field, the at least one bit formatter comprising (i) a gating circuit to gate the control signal using the mask bit, and (ii) a selector circuit coupled to the gating circuit to select one of a bit at the bit position of the shifted operand, the shift carry operand, and a most significant bit of the operand based on the gated control signal.

2. (Canceled).

3. (Previously presented) The apparatus of claim 1 wherein the control signal is one of a zero extension signal, a sign extension signal, and a use shift carry signal.

4. (Previously presented) The apparatus of claim 3 wherein when the mask bit is negated, the corresponding bit in the shifted operand is passed through unmodified.

5. (Previously presented) The apparatus of claim 3 wherein when the mask bit is asserted, the corresponding bit in the shifted operand is operated upon according to the control signal.

6. (Canceled).

7. (Currently amended) The apparatus of claim [[6]] 1 wherein the selector circuit selects the bit at the bit position of the shifted operand when the mask bit is negated.

8. (Currently amended) The apparatus of claim [[6]] 1 wherein the selector circuit selects the bit at the bit position of the shifted operand when the mask bit is asserted, the zero extension signal is asserted, the sign extension signal is negated, and the use shift carry signal is negated.

9. (Currently amended) The apparatus of claim [[6]] 1 wherein the selector circuit selects the bit at the bit position of the shift carry operand when the mask bit is asserted and the use shift carry signal is asserted.

10. (Currently amended) The apparatus of claim [[6]] 1 wherein the selector circuit selects the most significant bit when the mask bit is asserted, the zero extension signal and the use shift carry signal are negated, and the sign extension signal is asserted.

11. (Currently amended) A method comprising:

shifting an operand according to an offset parameter, generating a shifted operand;

storing the shifted operand in a register capable of transferring a shift carry operand stored in the register before storing the shifted operand; and

processing the shifted operand to generate an output based on at least a control signal and a mask field by a processing method comprising decoding the offset parameter into the mask field, the mask field having a plurality of mask bits, each of the mask bits corresponding to a bit position of the shifted operand, wherein processing the shifted operand comprises (i) gating the control signal using the mask bit, and (ii) selecting one of a bit at the bit position of the shifted operand, the shift carry operand, and a most significant bit of the operand based on the gated control signal.

12. (Canceled).

13. (Previously presented) The method of claim 11 wherein the control signal is one of a zero extension signal, a sign extension signal, and a use shift carry signal.

14. (Previously presented) The method of claim 13 wherein when the mask bit is negated, the corresponding bit in the shifted operand is passed through unmodified.

15. (Previously presented) The method of claim 13 wherein when the mask bit is asserted, the corresponding bit in the shifted operand is operated upon according to the control signal.

16. (Canceled).

17. (Currently amended) The method of claim [[16]] 11 wherein selecting comprises selecting the bit at the bit position of the shifted operand when the mask bit is negated.

18. (Currently amended) The method of claim [[16]] 11 wherein selecting comprises selecting the bit at the bit position of the shifted operand when the mask bit is asserted, the zero extension signal is asserted, the sign extension signal is negated, and the use shift carry signal is negated.

19. (Currently amended) The method of claim [[16]] 11 wherein selecting comprises selecting the bit at the bit position of the shift carry operand when the mask bit is asserted and the use shift carry signal is asserted.

20. (Currently amended) The method of claim [[16]] 11 wherein selecting comprises selecting the most significant bit when the mask bit is asserted, the zero extension signal and the use shift carry signal are negated, and the sign extension signal is asserted.

21. (Currently amended) A processing unit comprising:

a register file having a plurality of registers, each of the ~~register~~ registers storing an operand;

an instruction decoder to decode an instruction; and

a shift processing unit coupled to the register file and the instruction decoder to perform an operation on the operand, the shift processing unit comprising:

a shift post processor;

a shifter to shift an operand according to an offset parameter, generating a shifted operand; and

a register coupled to the shift post processor capable of transferring a shift carry operand stored in the register to the shift post processor, and coupled to the shifter to store the shifted operand after any transfer of the shift carry operand;

wherein the shift post processor is coupled to the shifter and the register to process the shifted operand to generate an output based on at least a control signal and a mask field, and

wherein the shift post processor comprises

a decoder to decode the offset parameter into the mask field, the mask field having a plurality of mask bits, each of the mask bits corresponding to a bit position of the shifted operand, and

at least one bit formatter coupled to the decoder to format the shifted operand using the control signal and the mask field, the at least one bit formatter comprising (i) a gating circuit to gate the control signal using the mask bit, and (ii) a selector circuit coupled to the gating circuit to select one of a bit at the bit position of the shifted operand, the shift carry operand, and a most significant bit of the operand based on the gated control signal.

22. (Canceled).

23. (Previously presented) The processing unit of claim 21 wherein the control signal is one of a zero extension signal, a sign extension signal, and a use shift carry signal.

24. (Previously presented) The processing unit of claim 23 wherein when the mask bit is negated, the corresponding bit in the shifted operand is passed through unmodified.

25. (Previously presented) The processing unit of claim 23 wherein when the mask bit is asserted, the corresponding bit in the shifted operand is operated upon according to the control signal.

26. (Canceled).

27. (Currently amended) The processing unit of claim [[26]] 21 wherein the selector circuit selects the bit at the bit position of the shifted operand when the mask bit is negated.

28. (Currently amended) The processing unit of claim [[26]] 21 wherein the selector circuit selects the bit at the bit position of the shifted operand when the mask bit is asserted, the zero extension signal is asserted, the sign extension signal is negated, and the use shift carry signal is negated.

29. (Currently amended) The processing unit of claim [[26]] 21 wherein the selector circuit selects the bit at the bit position of the shift carry operand when the mask bit is asserted and the use shift carry signal is asserted.

30. (Currently amended) The processing unit of claim [[26]] 21 wherein the selector circuit selects the most significant bit when the mask bit is asserted, the zero extension signal and the use shift carry signal are negated, and the sign extension signal is asserted.

31. (Previously presented) The apparatus of claim 3, wherein the use shift carry signal instructs the shift post processor to process the shifted operand based on the shift carry operand.

32. (Previously presented) The method of claim 12, wherein, in response to the use shift carry signal, the processing step is based on a shift carry operand transferred from the register before the shifted operand is stored in the register.

33. (Previously presented) The processing unit of claim 23, wherein the use shift carry signal instructs the shift post processor to process the shifted operand based on the shift carry operand.